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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/654,875	09/05/2000	Isao Nojiri	50006-073	7618

7590 03/08/2004

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/654,875	NOJIRI ET AL.
	Examiner	Art Unit
	Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-10 and 13-21* is/are pending in the application.

4a) Of the above claim(s) *7-9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10 and 13-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *19*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 17 is rejected under 35 U.S.C. 102(e) as being anticipated by Fukui et al. (US Pat. 6100594).

Regarding claim 17, Fukui et al. disclose a semiconductor device (Fig. 4-9B) comprising:

- a circuit board (Col. 6, line 31; see 5 in Fig. 4)
- a first semiconductor chip (1 in Fig. 7b/7a-9b) positioned on the circuit board
- a second semiconductor chip (1 in Fig. 7b/7a-9b) positioned on the first semiconductor chip
- the circuit board has a first pad and a second pad (see fourth and sixth pad 13 respectively from left in Fig. 7b), the second pad being spaced away from the first pad in a direction along an outer periphery/side of the first semiconductor chip (see fourth and sixth pad 13 from the left being connected with short wires 7 to respective pads 17a on the chip 1 in Fig. 7b)

- the first semiconductor chip has a third pad, a fourth pad spaced away from the third pad (see third and fourth pad 17a respectively from left on the chip 1 in Fig. 7b) in a direction along an outer periphery/side of the second semiconductor chip, the third and fourth pads being positioned adjacent to the first and second pads, respectively
- the second semiconductor chip has a fifth pad (see third pad 17b from left on the chip 2 in Fig. 7b) positioned adjacent to the third pad but away from the fourth pad on the first semiconductor chip, and
- the first pad on the circuit board and the third pad on the first semiconductor chip and the second pad on the circuit board and the fourth pad on the first semiconductor chip are electrically connected through respective bonding wires (see 7 in Fig. 7b) and the first pad on the circuit board and the fifth pad on the second semiconductor chip being connected through two bonding wires (see 7 in Fig. 7b).

Fig. 7b; Fig. 4-9b; Col. 10, lines 30-67; Col. 6-10).

Fukui et al. further teach:

- the first pad on the circuit board and the fifth pad on the second semiconductor chip being connected through a single bonding wire (see a long wire 7 connecting pads 13 and 17b in Fig. 7a), and

- a wire/trace being extended along the outer periphery of the second semiconductor chip between two pads (see the wire/trace connecting pads 17a in Fig. 9b), such wire/trace on the circuit board being printed/patterned using a conventional metal deposition and photolithography/printing processes (Col. 7, line 30-60).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

4. Claims 10 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (APA) in view of Fukui et al. (US Pat. 6100594) and Kozono (US Pat. 5399904).

Regarding claims 10 and 13, APA teaches a conventional semiconductor device (Fig. 11 and 12) comprising:

- a circuit board (CB) having an outer periphery/perimeter (see 102 in Fig. 11/12)

- a first semiconductor chip (110 in Fig. 11/12) positioned on the circuit board, the first chip being configured to be smaller than the circuit board so that it is confined within an outer periphery/perimeter of the circuit board
- a second semiconductor chip (112 in Fig. 11/12) positioned on the first semiconductor chip, the second chip being configured to be smaller than the first chip so that it is confined within an outer periphery/perimeter of the first chip
- the circuit board has a pad/second pad (104-1 in Fig. 12)
- the second semiconductor chip (112 in Fig. 12) has a pad/third pad (114-1 in Fig. 12), positioned closer/adjacent to the second pad
- the second pad on the circuit board and the third pad on the second chip are electrically connected through a bonding wire (116 in Fig. 11/12), and
- the device having the CB being conventionally mounted on a motherboard (APA, pages 1-4)

(APA: Fig. 11 and 12; specification pages 1-4).

The APA fails to teach:

- the circuit board having a first pad such that the second pad is spaced away from the first pad in a direction along the outer periphery of the chip, and
- the circuit board further having a wire connecting the first and second pads, the wire being printed on the circuit board together with the first and second pads

and being extended along the outer periphery of the first chip between the first and second pads.

Kozono teaches a circuit board substrate having an array of bonding/connection pads (see 22 in Fig. 2) such that the bonding/connection pads are spaced from each other along outer periphery/peripheral edges of a chip (see configuration of 23 with respect to a bonding site 24 in Fig. 2), the spaced bonding/connection pads further being connected by a conducting metal/wiring layer/trace to provide the array/configuration suitable for wire boding respective pads along peripheral portions of the chip (Col. 2, lines 42-63).

Fukui et al. teach forming a wiring portion/trace pattern on a circuit board/substrate using conventional metal deposition and photolithography/printing processes (Col. 7, line 30-60).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the circuit board having a first pad such that the second pad is spaced away from the first pad in a direction along the outer periphery of the chip and the circuit board further having a wire connecting the first and second pads, the wire being printed on the circuit board together with the first and second pads and being extended along the outer periphery of the first chip between the first and second pads as taught by Kozono and Fukui et al. so that the bonding wire density can be increased and wire bonding defects can be reduced in the APA.

Regarding claims 14 and 15, APA, Kozono and Fukui et al. teach substantially the entire structure as applied to claim 10 above, wherein APA and Kozono further teach the circuit board having additional pads including fourth and fifth pads being positioned adjacent/near the outer periphery/perimeter of the first chip (see APA: pads 114-2 on the chip 110 in Fig. 12; Kozono: the array/configuration of 22 in Fig. 2).

Regarding claim 16, APA, Kozono and Fukui et al. teach substantially the entire structure as applied to claim 10 above, wherein APA further teaches the second chip having a sixth pad being positioned adjacent/near the outer periphery/perimeter of the second chip (see APA: 114-3 in Fig. 12).

5. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukui et al. (US Pat. 6100594) in view of the APA.

Regarding claim 18, Fukui et al. teach the entire structure as applied to claim 17 above, except the semiconductor device being mounted on a motherboard.

APA teaches the device having the circuit board being conventionally mounted on a motherboard (APA, specification pages 1-4).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the semiconductor device being mounted on the

motherboard as taught by APA so that component density can be increased in Fukui et al's device.

6. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukui et al. (US Pat. 6100594) in view of Lee et al. (US Pat. 5606196).

Regarding claim 19, Fukui et al. disclose a semiconductor device (Fig. 4-9B) comprising:

- a circuit board (Col. 6, line 31; 5 in Fig. 4)
- a first semiconductor chip (1 in Fig. 7b/7a-9b) positioned on the circuit board
- a second semiconductor chip (2 in Fig. 7b/7a-9b) positioned on the first semiconductor chip
- the circuit board has a first pad and a second pad (see sixth and seventh pad 13 respectively from left in Fig. 7b), the second pad being spaced away from the first pad in a direction along an outer periphery/side of the first semiconductor chip
- the second semiconductor chip has a third pad (see fifth pad 17b from left on the chip 2 in Fig. 7b) positioned adjacent to the second pad but away from the first pad on the circuit board, and

- the second pad on the circuit board and the third pad on the second semiconductor being electrically connected through a bonding wire (see 7 in Fig. 7b).

(Fig. 7b; Fig. 4-9b; Col. 10, lines 30-67; Col. 6-10).

Fukui et al. fail to teach the first and second pads on the circuit board being electrically connected through a bonding wire.

Lee et al. teach a high density chip package (HDCP) where a single or a plurality of bonding/screening wires are used to provide an electrical connection between bonding sites/bonding pads on a printed wiring board (see 88 on the PWB 80 in Fig. 8A/8B) or a chip respectively (Col. 7, lines 46-55) and to reduce mutual inductance and cross talk in the wire bonded HDCP (Col. 6, lines 1-5; Col. 7, lines 22-38).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first and second pads on the circuit board being electrically connected through the bonding wire as taught by Lee et al. so that mutual inductance and cross-talk can be reduced in Fukui et al's device.

Regarding claim 20, Fukui et al. and Lee et al. teach substantially the entire structure as applied to claim 19 above, wherein Fukui et al. teach the first semiconductor chip having a plurality of pads being positioned adjacent the outer periphery/side of the first semiconductor chip including a sixth pad (see 17a at the farthest right in Fig. 7b).

7. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukui et al. (US Pat. 6100594) and Lee et al. (US Pat. 5606196) as applied to claim 19 above, and further in view of the APA.

Regarding claim 21, Fukui et al. and Lee et al. teach the entire structure as applied to claim 19 above, except the semiconductor device being mounted on a motherboard.

APA teaches the device having the circuit board being conventionally mounted on a motherboard (APA, specification pages 1-4).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the semiconductor device being mounted on the motherboard as taught by the APA so that component density can be increased in Lee et al. and Fukui et al's device.

Response to Arguments

8. Applicant's arguments with respect to claim 10 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

Nitin Parekh
02-25-04

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